

AMENDMENTS TO CLAIMS:

The listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (currently amended) A method for high speed addressing of a memory space having 2^M addresses using an N-bit bus, where M is greater than N, comprising the steps of:

(a) providing at least two registers, each register to store a distinct N-bit address-byte of a plurality of address-bytes that together define an address in the memory space, each register associated with a particular count of address-bytes received on the bus;

(b) receiving a first address-byte on the bus~~one byte of a plurality of N-bit bytes that together define an address in the memory space;~~

(c) producing a first count of address-bytes received on the bus as a result of receiving the first address-byte~~incrementing a count as a result of completing step (b);~~

(d) selecting a first one of the at least two registers, the first register corresponding with the first count~~addressing one of said two registers according to the incremented count in step (c); and~~

(e) storing the first address-byte in the selected first register~~storing said one byte in the register addressed in step (d).~~

2. (currently amended) The method of claim 1, further comprising:

receiving a second address-byte;~~receiving another byte of said plurality of bytes;~~

producing a second count of address bytes received on the bus as a result of receiving the second address-byte;~~resetting the count from step (c);~~

selecting a second one of the at least two registers, the second register corresponding with the second count;~~addressing the other of said two registers as a result of the reset count; and~~

~~storing the second address-byte in the selected second register—storing said other-byte in said other-register.~~

3. (currently amended) The method of claim 2, further comprising the steps of:

(a) receiving a memory access command; and

(b) accessing the memory space at an said address defined by the first and second address-bytes as a result of ~~based on the said~~ memory access command.

4. (currently amended) The method of claim 3, wherein the said memory access command is a write ~~data~~ command.

5. (currently amended) The method of claim 3, wherein the said memory access command is a read ~~data~~ command.

6. (currently amended) The method of claim 3~~1~~, wherein the second address-byte is received in a next subsequent bus transaction following receipt of the first address-byte. ~~further comprising receiving another byte of said plurality of bytes, incrementing the count from step (c) to obtain a next incremented count, addressing the other of said two registers as a result of the next incremented count, and storing said other byte in said other register.~~

7. (currently amended) The method of claim 6, wherein the memory access command is received in a next subsequent bus transaction following receipt of the second address-byte. ~~further comprising the steps of:~~

~~(a) receiving a memory access command; and~~

~~(b) accessing the memory space at said address based on said memory access command.~~

8. (cancelled)

9. (cancelled)

10. (currently amended) The method of claim 1, further comprising a step of providing a memory. wherein the said 2^M address memory space comprises the address space of the a-memory-device.

11. (currently amended) The method of claim 1, further comprising a step of providing at least two memories. wherein the said 2^M address memory space

comprises the address space of the at least two memories ~~a plurality of memory devices.~~

12. (currently amended) An apparatus for high speed addressing of a memory space having 2^M addresses ~~using an N-bit bus, where M is greater than N,~~ comprising:

(a) at least two registers, each register to store a distinct N-bit address-byte of a plurality of address-bytes that together define an address in the memory space, each register associated with a particular count of address-bytes received on the bus;

(b) an N-bit bus, where M is greater than N ~~a counter; and~~

(c) a logic circuit coupled with the bus and the at least two registers, the logic circuit to select one of the at least two registers, the logic circuit including: ~~adapted for:~~

(i) an address-byte-received counter to count address-bytes received on the bus; and receiving one byte of a plurality of N-bit bytes that together define an address in the memory space;

(ii) a selecting unit to select one of the at least two registers according to the count of the address-byte-received counter, wherein the selecting unit selects a distinct one of the at least two registers for a particular count value of the address-byte-received counter, incrementing a count of said counter as a result of completing step (i);

(iii) ~~addressing one of said two registers according to the incremented count in step (ii); and~~

(iv) ~~storing said one byte in said register addressed in step (iii).~~

13. (currently amended) The apparatus of claim 12, wherein the said logic circuit stores a received address-byte in a selected one of the at least two registers, ~~is further adapted for receiving another byte of said plurality of bytes, resetting the count of said counter, addressing the other of said two registers as a result of the reset count, and storing said other byte in said other register.~~

14. (currently amended) The apparatus of claim 13, further comprising a unit to: ~~wherein said logic circuit is further adapted for:~~

(a) receive ~~receiving~~ a memory access command; and

~~(b)~~ access ~~accessing~~ the memory space at an ~~said~~ address defined by the first and second address-bytes as a result of ~~based on the~~ said memory access command.

15. (currently amended) The apparatus of claim 14, wherein the ~~said~~ memory access command is a write ~~data~~ command.

16. (currently amended) The apparatus of claim 14, wherein the ~~said~~ memory access command is a read ~~data~~ command.

17. (currently amended) The apparatus of claim ~~14~~13, wherein the ~~logic circuit receives a second address-byte in a next subsequent bus transaction following receipt of a first address-byte. said logic circuit is further adapted for receiving another byte of said plurality of bytes, incrementing the count of said counter to obtain a next incremented count, addressing the other of said two registers as a result of the next incremented count, and storing said other byte in said other register.~~

18. (currently amended) The apparatus of claim 17, wherein the ~~unit receives the memory access command in a next subsequent bus transaction following receipt of the second address-byte. said logic circuit is further adapted for:~~

~~(a) receiving a memory access command; and~~

~~(b) accessing the memory space at said address based on said memory access command.~~

19. (cancelled)

20. (cancelled)

21. (currently amended) The apparatus of claim 12, further comprising a memory, the addresses of which are defined by the 2^M address memory space. ~~wherein said 2^M address memory space comprises the address space of a memory device.~~

22. (currently amended) The apparatus of claim 12, further comprising at least two memories, the addresses of which are defined by the 2^M address memory space. ~~wherein said 2^M address memory space comprises the address space of a plurality of memory devices.~~

23. (currently amended) A machine readable medium embodying a program of instructions for execution by a machine to perform a method for high speed addressing of a memory space having 2^M addresses using an N-bit bus, the machine having at least two registers, each register to store a distinct N-bit address-byte of a plurality of address-bytes that together define an address in the memory space, each register associated with a particular count of address-bytes received on the bus, where M is greater than N, comprising the steps of:

- (a) receiving a first address-byte on the bus~~one byte of a plurality of N-bit bytes that together define an address in the memory space;~~
- (b) producing a first count of address-bytes received on the bus as a result of receiving the first address-byte~~incrementing a count as a result of completing step (a);~~
- (c) selecting a first one of the at least two registers, the first register corresponding with the first count~~addressing one of the at least two registers according to the incremented count in step (b); and~~
- (d) storing the first address-byte in the selected first register~~said one byte in the register addressed in step (c).~~

24. (currently amended) The machine readable medium of claim 23, the method further comprising the steps of:

- receiving a second address-byte;
- producing a second count of address-bytes received on the bus as a result of receiving the second address-byte;
- selecting a second one of the at least two registers, the second register corresponding with the second count; and
- storing the second address-byte in the selected second register. ~~-adapted so that the method further comprises receiving another byte of said plurality of bytes, resetting the count from step (c), addressing the other of said two registers as a result of the reset count, and storing said other byte in said other register.~~

25. (currently amended) The machine readable medium of claim 24, ~~adapted so that~~ the method further comprising ~~comprises~~ the steps of:

(a) receiving a memory access command; and

(b) accessing a memory at an address defined by the first and second address-bytes as a result of the memory space at said address based on said memory access command.

26. (currently amended) The machine readable medium of claim 25, ~~adapted so that wherein~~ the said memory access is a write data access.

27. (currently amended) The machine readable medium of claim 25, ~~adapted so that wherein~~ the said memory access is a read data access.

28. (currently amended) The machine readable medium of claim 25, ~~wherein the second address-byte is received in a next subsequent bus transaction following receipt of the first address-byte. 23 adapted so that the method further comprises receiving another byte of said plurality of bytes, incrementing the count from step (c) to obtain a next incremented count, addressing the other of said two registers as a result of the next incremented count, and then storing said other byte in said other register.~~

29. (currently amended) The method of claim 28, ~~wherein the memory access command is received in a next subsequent bus transaction following receipt of the second address-byte. 28, further comprising the steps of:~~

~~(a) receiving a memory access command; and~~

~~(b) accessing the memory space at said address based on said memory access command.~~

30. (cancelled)

31. (cancelled)

32. (currently amended) The machine readable medium of claim 23, wherein the 2^M address memory space comprises the address space of a memory. ~~wherein said 2^M address memory space comprises the address space of a memory device.~~

33. (currently amended) The machine readable medium of claim 23, wherein the 2^M address memory space comprises the address space of at least two

~~memories, wherein said 2^M -address memory space comprises the address space of a plurality of memory devices;~~

34. (cancelled)

35. (cancelled)

36. (cancelled)

37. (currently amended) ~~An system apparatus for high speed access of a memory space having 2^M addresses using an N-bit bus, where M is greater than N, comprising:~~

~~(a) an N-bit bus, where M is greater than N; at least two registers, wherein each of said registers contains one of a plurality of N-bit bytes that together define an address in the memory space; and~~

~~(b) a memory having 2^M addresses; a logic circuit adapted for receiving a memory access command that does not specify said registers, and accessing the memory space at said address as a result of said memory access command;~~

~~(c) a central processing unit, coupled with the bus, to transmit at least two address-bytes that together define an address in the memory space and to transmit a memory access command;~~

~~(d) at least two registers, each register to store a distinct N-bit address-byte of a plurality of address-bytes that together define an address in the memory, each register associated with a particular count of address-bytes received on the bus; and~~

~~(e) a logic circuit coupled with the bus and the at least two registers, the logic circuit to receive and store address-bytes in a selected one of the at least two registers, the logic circuit including:~~

~~(i) an address-byte-received counter to count address-bytes received on the bus;~~

~~(ii) a selecting unit to select one of the at least two registers according to the count of the address-byte-received counter, wherein the selecting unit selects a distinct one of the at least two registers for a particular count value of the address-byte-received counter; and~~

~~(f) a unit to:~~

(i) receive the memory access command; and

(ii) access the memory at an address defined by the first and second address-bytes as a result of the memory access command.

38. (currently amended) The system apparatus of claim 37, wherein said logic circuit is further adapted so that said the memory access command is a write command data access.

39. (currently amended) The system apparatus of claim 37, wherein said logic circuit is further adapted so that said the memory access command is a read command data access.

40. (currently amended) The system of claim 37, wherein the logic circuit receives a second address-byte in a next subsequent bus transaction following receipt of a first address-byte. A machine-readable medium embodying a program of instructions for execution by a machine to perform a method for high-speed access of a memory space having 2^M addresses using an N-bit bus, where M is greater than N, comprising the steps of:

(a) providing at least two registers, wherein each of said registers contains one of a plurality of N-bit bytes that together define an address in the memory space;

(b) receiving a memory access command that does not specify said registers; and

(c) accessing the memory space at said address as a result of said memory access command.

41. (currently amended) The system of claim 40, wherein the unit receives the memory access command in a next subsequent bus transaction following receipt of the second address-byte. The machine-readable medium of claim 40, wherein said method is adapted so that said memory access command is a write data command.

42. (currently amended) The system of claim 41, wherein the system comprises a cellular telephone. The machine-readable medium of claim 40, wherein said method is adapted so that said memory access command is a read data command.